

IN THE CLAIMS:

Amend the claims as indicated below.

1 Claim 83 (canceled)

1 84. (New) A content addressable memory (CAM) device comprising:
2 a plurality of CAM blocks, each comprising at least one storage partition, wherein a
3 storage partition comprises one or more configurable portions of one or more CAM blocks, and
4 wherein a class code specifies a particular storage partition;
5 a block select circuit coupled to the plurality of CAM blocks, wherein the block select
6 circuit receives a class code signal that indicates a storage partition that will participate in a CAM
7 operation and outputs a configuration signal to each of the plurality of CAM blocks that indicates
8 a CAM block configuration corresponding to the received class code signal; and
9 a plurality of block flag circuits each coupled to the block select circuit and to one of the
10 plurality of CAM blocks, wherein each block flag circuit receives a configuration signal and a
11 plurality of row flag signals, wherein the plurality of row flag signals indicate results of the CAM
12 operation on a row basis, and wherein each block flag circuit outputs a block flag signal that
13 indicates a result of the CAM operation within the coupled CAM block for the storage partition
14 indicated by the class code signal.

1 85. (New) The CAM device of claim 84, wherein the block select circuit further outputs a
2 block select signal for each of the plurality of CAM blocks, wherein the block select signal
3 indicates whether a CAM block is part of the storage partition indicated by the class code signal.

1 86. (New) The CAM device of claim 85, wherein if the CAM block is not part of the
2 storage partition indicated by the class code signal, the CAM block does not participate in the
3 CAM operation and block flag signal does not indicate a result of the CAM operation within the
4 coupled CAM block.

1 87. (New) The CAM device of claim 84, further comprising:
2 an operation select signal received by each of the block flag circuits that indicates the
3 CAM operation to be performed, wherein the CAM operation comprises,
4 comparing at least one segment of each row to a comparand value; and
5 signaling, using a block flag signal coupled to a CAM block, a block match condition
6 for the CAM block and class code if at least one comparison results in a match.

1 88. (New) The CAM device of claim 87, further comprising a global flag encoder circuit
2 coupled to receive block flag signals from each of the plurality of CAM blocks, wherein when a
3 block match condition is indicated for any of the plurality of CAM blocks having a same class
4 code, the global flag encoder circuit outputs a device flag signal indicating the match condition.

1 89. (New) The CAM device of claim 84, further comprising:
2 an operation select signal received by each of the block flag circuits that indicates the
3 CAM operation to be performed, wherein the CAM operation comprises,
4 examining valid signals for all segments of a CAM block coupled to a block flag
5 circuit;
6 signaling, using a row flag signal, that a row is full when all the segments of a row

7 have valid entries; and

8 signaling, using a block flag signal, the CAM block is full when the row flags coupled
9 to the CAM block indicate all rows are full.

1 90. (New) The CAM device of claim 89, further comprising a global flag encoder circuit
2 coupled to receive block flag signals from each of the plurality of CAM blocks, wherein when all
3 CAM blocks with a same class code are indicated to be full, the global flag encoder circuit
4 outputs a device flag signal indicating a full condition.

1 91. (New) The CAM device of claim 84, wherein the CAM block configuration
2 comprises a block width and a block depth.

1 92. (New) A content addressable memory (“CAM”) device comprising:
2 a plurality of CAM blocks comprising a plurality of configurable storage partitions,
3 wherein a storage partition is specified by a class code;
4 a block select circuit that receives a class code signal indicating a class code of a storage
5 partition that will participate in a CAM operation and generates a configuration signal for each
6 CAM block, wherein the configuration signal indicates a storage partition configuration
7 corresponding to the class code; and
8 a plurality of block priority encoder circuits each coupled to one of the plurality of CAM
9 blocks, wherein a block priority encoder circuit coupled to a CAM block receives a configuration
10 signal for the coupled CAM block and generates a block index for the coupled CAM block that
11 indicates a CAM address in the coupled CAM block based on the CAM operation performed and
12 on the class code.

1 93. (New) The CAM device of claim 92, further comprising a global priority encoder
2 circuit that receives a plurality of block indices and a plurality of block flag signals, wherein a
3 block flag signal indicates a result of the CAM operation performed, and wherein the global
4 priority encoder outputs a device index that indicates a CAM address in one of the plurality of
5 CAM blocks based on the CAM operation performed and on the class code.

1 94. (New) The CAM device of claim 92, wherein the CAM operation comprises:
2 a compare operation, wherein the block index indicates a match address; and
3 a write operation, wherein the block address indicates a free address.

1 95. (New) The CAM device of claim 94, wherein:
2 when the CAM operation is a compare operation, the device index indicates a highest
3 priority match address; and
4 when the CAM operation is a write operation, the device index indicates a next free
5 address.

1 96. (New) The CAM device of claim 92, wherein each of the plurality of block priority
2 encoders further comprises a main priority encoder that monitors row flag signals that indicate a
3 result of the CAM operation on a row segment basis.

1 97. (New) The CAM device of claim 96, wherein when the CAM operation is a compare
2 operation, the main priority encoder monitors row flag signals to generate a row address that
3 corresponds to an address of a highest priority row of a CAM block having at least one row
4 segment that matches the comparand.

1 98. (New) The CAM device of claim 97, wherein when the CAM operation is a write
2 operation, the main priority encoder monitors row flag signals to generate a row address that
3 corresponds to an address of a highest priority row of a CAM block that has at least one row
4 segment that is not full.

1 99. (New) The CAM device of claim 98, wherein the block priority encoder further
2 comprises select logic that receives the row address generated by the main priority encoder and
3 the configuration signal, and selects a segment address associated with a row of CAM cells
4 specified by the address of the highest priority row, and generates the block index.

1 100. (New) The CAM device of claim 92, wherein the configurable storage
2 partitions are configurable into at least a specified width and a specified depth.